each inverter, B1 and B2. In this embodiment, the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and the [a] dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors, each driven by one of the dual gates. In this embodiment, the drain regions, 204 and 212, for one of the cross-coupled inverters, B1, is further coupled to a gate of the transistor of the first conductivity type, M2, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2. Similarly, the drain regions, 206 and 214, for inverter, B2, is coupled to a gate of the transistor of the first conductivity type, M1, and to a second gate of the dual-gated MOSFET in the other one of the cross-coupled inverters, B1 and B2.

Applicant respectfully submits that the nomenclature for the pair of transistors M3, M5, and M4, M6 as dual-gated MOSFETs is appropriate in the circumstances under which the nomenclature is used. Applicant is allowed to define terms in his application in a manner that he deems best to describe his invention. Applicant may be his or her own lexicographer as long as the meaning assigned to the term is not repugnant to the term's well known usage. M.P.E.P. 2111.01 citing *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). In the specification page 9 lines 3-4, the transistor pairs M3, M5 and M4, M6 are configured such that the drains of M3 and M5 are coupled and the drains of M4 and M6 are coupled. In the specification page 9 lines 5-6, the transistor pairs M3, M5 and M4,M6 are configured such that the sources of M3 and M5 are coupled and the sources of M4 and M6 are coupled. Therefore, M3 and M5 are transistors configured to be in parallel as are transistors M4 and M6. (Note that this is also indicated in the original drawing). The specification, on page 10 line 22, further discloses an embodiment in which the transistors M3 and M5 (M4 and M6) are "a dual-gated MOSFET", clearly meaning a single MOSFET, which the Applicant has called "a dual-gated metal oxide semiconductor field effect transistor (MOSFET)." As an embodiment of the disclosure given earlier on page 9, this MOSFET must have the drains of M3 and M5 (M4 and M6) coupled and the sources M3 and M5

(M4 and M6) coupled. Further, the specification on page 10 line discloses each transistor, M3 and M5, (M4 and M6) is "driven by one of the dual gates." The term dual-gated MOSFET clearly describes the transistor pair M3, M5 (M4, M5) as a MOSFET with two transistors in parallel having two gates as taught in the application including the claims.

Though the Examiner has long held that it "is well known in the art that dual-gated transistor is a two series connected transistors," the Examiner has failed to provide a reference supporting his long held belief that only series connected transistors are referred to as dual-gated transistors. A publication issued prior to the filing date of the instant application describes a SOI P-MOSFET which uses two gates in a parallel structure. See, Denton, J.P. et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate," IEEE Electron Device Letters, 17(11),509-511,(Nov.1996) that was cited in the 6,104,068 patent. Other publications referring to a single MOSFET having two transistors in parallel with two gates as a dual-gate MOSFET include Mizuno, T. et al., "High Performance Characteristics in Trench Dual-Gate MOSFET (TDMOS)," IEEE Transactions on Electron Devices, 138(9),2121-2127,(Sept.1991), and Frank, D.J. et al., "Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?," IEDM TECHNICAL DIGEST: INTERNATIONAL ELECTRON DEVICES MEETING, 21.1.1-21.1.4, (Dec.1992). These exemplary publications substantiate that Applicant's use of the term dual-gated MOSFET in the manner in which he defines it in the instant application would be understood by one skilled in the art upon reading the specification. Obviously, given that MOSFETs with parallel connected transistors and two gates have been referred to as dual-gated MOSFETs by others, Applicant's use of the term dual-gated MOSFET is not repugnant to the term's well known usage. In light of this discussion, Applicant respectfully submits that the term dual-gated MOSFET is descriptive of his inventive entity and respectfully requests that the Office Action objection to dual-gated MOSFET in the specification be withdrawn.